The NI Electronics Education Platform: A Case Study

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Overview

This application note details how instructors can use an integrated laboratory to enhance their electronics courses. We begin by outlining a typical method for teaching circuits, and continue with a discussion of the elements of the integrated laboratory and how it can solve many of the challenges that students must face when conducting laboratory experiments, bridging the gap between theory and the real-world. Through a detailed case study using an actual experiment used in a recognized University, we see first hand the benefits that an integrated solution provides.

Throughout institutions world-wide, the approach to teaching electronics has generally remained the same for many years. Students learn circuit theory by participating in lectures, and gain a deeper fundamental understanding through complimentary experiments. The laboratory experiment presents a design challenge that requires students to apply theory from lectures using hand calculations, conduct simulations, create and measure their designs, and then compare their results with expected values. All of this work culminates in a deliverable report, detailing the student's experience.

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1. Benefits of the Integrated Solution

The integrated platform provides an uninterrupted flow of data from simulation to prototyping and measurement, bridging the gap between theory and hands-on learning. This platform will allow students quick and easy access to measurements. Through instruments in the simulated environment students gain a better understanding of the purpose simulation, and how to use the results they get when evaluating real circuitry.

An integrated laboratory presents a unified platform for simulation, prototyping, measurement and comparison. With a consistent approach and the power of computer-based measurement, students will quickly and easily understand how to develop their schematics, carry out powerful simulations, and take important measurements.

A great amount of time is spent while students try to compare measured data with simulation. Frequently measurements taken using sophisticated instruments are transcribed manually and entered into a spreadsheet for analyses. Much time is spent on the logistics of comparison rather than trying to understand why differences exist.

National Instruments and Electronics Workbench are committed to providing a powerful integrated solution for electronics education. The platform currently consists of Electronics Workbench Multisim for schematic capture and SPICE simulation, National Instruments ELVIS for prototyping, and LabVIEW and SignalExpress for measurement and comparison. Figure 1 below illustrates the integrated laboratory.

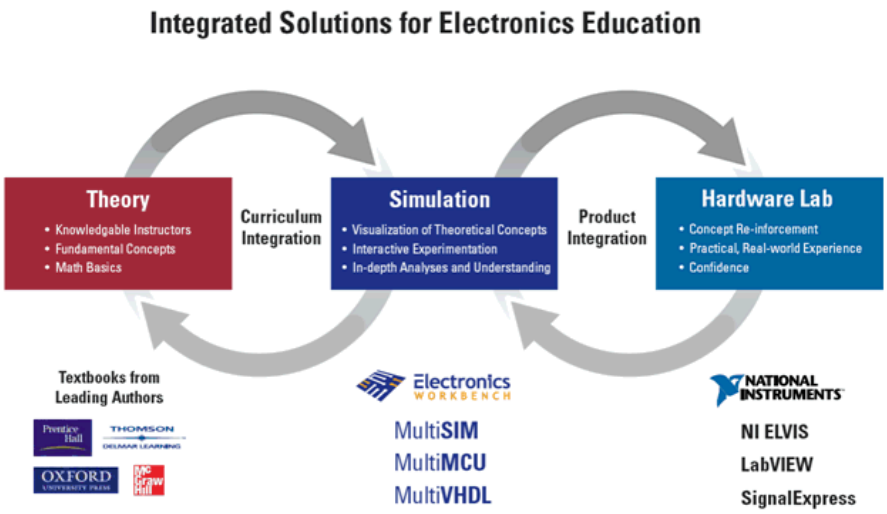


Figure 1. A Conceptual View of the Integrated Platform

With the power and flexibility provided by Multisim, students gain the advantages of an industry-caliber, easy-to-use circuit simulator. Multisim includes powerful virtual instruments, which are simulated instruments found in the lab such as oscilloscopes, multimeters, function generators, among many others. These instruments provide students with a fast and intuitive method for obtaining simulation results while preparing them for the instruments they will use in the lab. Figure 2 below shows an example screen capture of the Multisim environment.

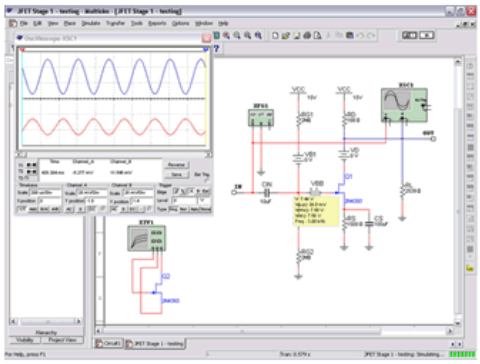


Figure 2. Multisim Schematic to take Simulated Measurements

Multisim is rich with features invaluable to academia such as rated components that will break should their maximum values are exceeded and interactive components whose values can be changed while the simulation is running.

Experimental prototypes are typically built on solder-less breadboards. Students must rely on datasheets and visual inspection to ensure that their prototypes will function correctly. A significant amount of time is often spent by lab instructors and teaching assistants correcting simple wiring mistakes – there is a need for a computer-aided prototyping tool. Multisim delivers a 3D virtual breadboarding environment. Students will learn prototyping through a virtual NI ELVIS breadboard that gives feedback on completion and correctness. The virtual environment looks and feels exactly like the real NI ELVIS workstation.

The NI ELVIS workstation contains several built-in instruments to carry-out measurements on prototyped circuits. The workstation comes equipped with a removable prototyping board, and connects directly to the PC to communicate measurements to a common interface. The instruments such as an oscilloscope and bode analyzer are easy-to-use and function just like traditional bench-top instruments. Figure 3 below shows the NI ELIVS system.

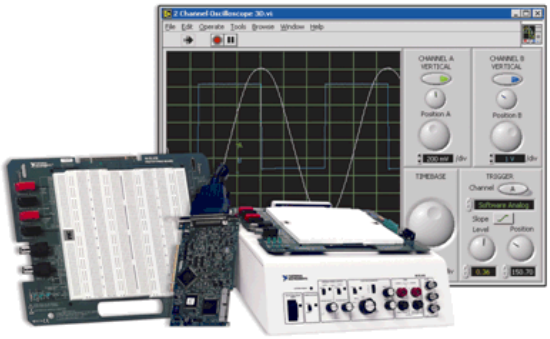


Figure 3. The NI ELVIS Workstation

The virtual instruments also allow for quick automated measurements to be taken. Using NI SignalExpress and LabVIEW, all measurements are available in a single environment, and can easily be saved and compared with simulations from Multisim on the same graph.

2. Case Study: The Laboratory Amplifier Design Project

To best illustrate the advantages of using the integrated laboratory, we consider a portion of an actual lab taught at the University of Alberta in Canada. We conduct the lab experiment using the integrated platform. We use Multisim to develop our circuit schematics and verify calculations through SPICE simulation, and the virtual 3D NI ELVIS prototyping environment within Multisim to virtually build and check our circuit. We then construct the circuit using real components placed the NI ELVIS breadboard, and take measurements with NI LabVIEW and SignalExpress. Finally, we complete the experiment with comparisons between measurements and simulations.

The objective of this lab is to design, build, and test an audio amplifier that provides a voltage gain of |150| ±10% at a design frequency of 3 kHz, with input impedance of greater than or equal to 1 MΩ. The amplifier load consists of a 1200:8 Ω matching transformer driving an 8 Ω speaker. The power supply voltage in this case will be the +15 volts DC supplied by the NI ELVIS.

The prospective design is a 3-stages process of common-emitter and common-source amplifiers: A JFET used on the input stage, to meet the high input impedance requirement, followed by two stages of common-emitter BJT amplifiers to satisfy the high gain requirements. A block diagram captured in Multisim illustrating the design is shown in Figure 4 below. The capacitors between stages provide DC isolation between the small signal inputs and outputs and the DC quiescent points of the circuit. Although the figure below shows the speaker and transformer, our simulations will use a simple load resistance in place of the transformer and speaker for simplicity's sake.

Note: All circuit diagrams were taken as screen shots directly from Multisim using the **Capture Screen Area** feature, located on the **Tools** menu.

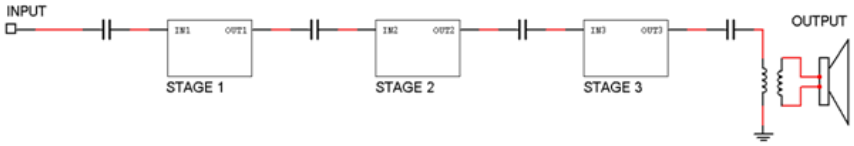


Figure 4. Amplifier Block Diagram

System gain is given by:

$$A_{V\_TOTAL} = A_{V\_STAGE\_1} A_{V\_STAGE\_2} A_{V\_STAGE\_3}$$

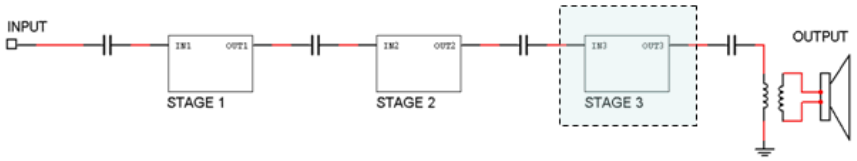
Since the voltage gain of each stage is dependent on the load resistance of that stage, and since the load resistance at each stage is determined by the components of the following stage, then it is best to work backwards from the final stage to the first stage in order to have the RL of each stage of interest. The load resistance of the last gain stage is a given known quantity, equal to 1200 Ω. We will use two 2N4401A general purpose NPN BJT transistors for the second and third stages and one 2N4393 JFET for the first input stage due to its high input impedance. Throughout the design we will verify hand calculations with Multisim, and include screen captures of results wherever applicable. We also use Multisim to determine through simulation the transconductance of the amplifiers to help us calculate gain, and for determining the DC load line which will help for biasing the amplifiers.

Practical and Simulation Considerations

Practically speaking, we acknowledge that the tolerances of components throughout the design will inevitably result in real world results that are different than predicted. Additionally, we are designing an audio amplifier, so it would be nice to have some method for controlling the gain (volume) manually. To both compensate for component tolerances, and to provide a manual volume control, we will include a variable resistor (potentiometer) in one of our amplifiers. We will choose to put this potentiometer in the parallel with RB1 of the second stage because this will provide a good range of variation in gain, while maintaining solid operating characteristics.

Often theoretical values do not have real world counterparts. Bearing this in mind, real components values are chosen that are as close as possible to the calculated values.

3. BJT Amplifier, Stage 3



For both the third and second stages, we will use the common emitter BJT amplifier topology shown below in Figure 5.

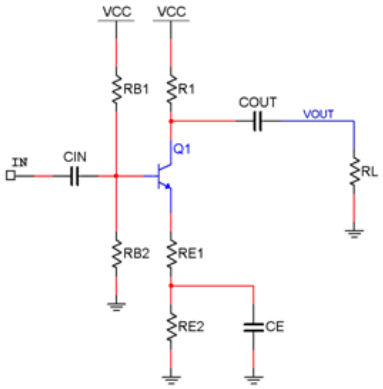


Figure 5. Common Emitter BJT Amplifier Stage with Load Resistance

In this configuration, CIN and COUT provide DC isolation between stages of the design. The capacitor CE creates a practical short at higher frequencies, effectively bypassing RE2. RB1 and RB2 create a voltage divider, providing the necessary voltage at the base to forward-bias the base-emitter junction of the transistor. RC, RE1, and RE2 create appropriate biasing conditions for an ideal combination of AC swing, voltage gain, and transistor stability in the active region.

Biasing

One of the most important aspects of amplifier design is to appropriately bias the transistors. Proper biasing ensures that the transistor will remain stable in the active region, and provide true gain without saturating the transistor and without distorting the input signal.

We take a practical approach in design using Multisim simulation to determine quiescent operating conditions and the component values that will provide a satisfactory stability, swing, and gain. To this end we will create a DC load line for component value selection. This is done using a curve trace of the transistor.

Multisim provides a virtual curve tracer for investigating transistor characteristics. The first step is to connect the curve tracer to the 2N4401 transistor used in this lab as shown in Figure 6 below. The tracer settings and results are shown in Figure 7 and Figure 8 below.

Note the Y-Intercept of the load line is equal to VCC/RC. When building the actual circuit using both Multisim and real components, we split this calculated value among RC RE1, and RE2.

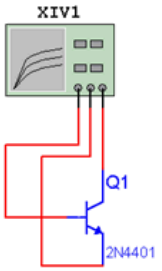


Figure 6. 2N4401 Curve Tracer Circuit

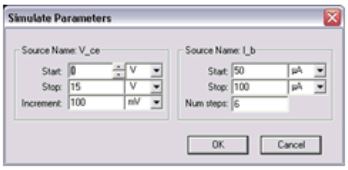


Figure 7. 2N4401 Curve Trace Settings

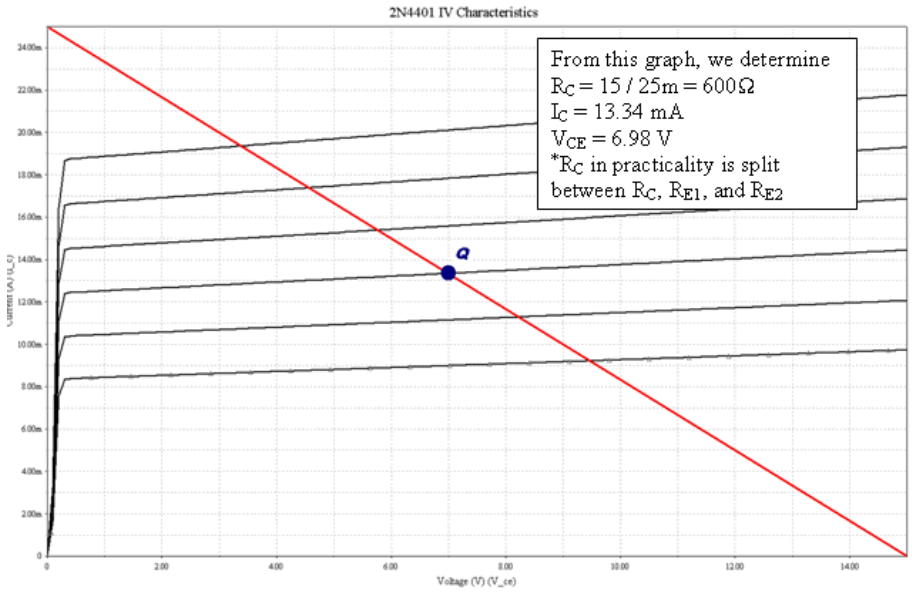


Figure 8 - 2N4401 Simulated Curve Trace with DC Load Line and Quiescent Point

In this case, the Q point has been chosen to provide optimal biasing conditions. The Q point is sufficiently to the right side of the graph to prevent the input signal from causing the transistor to saturate, yet far enough to the left to prevent clipping the output at 15 V, which is the maximum supply voltage VCC. For a common emitter circuit with no emitter resistance at high frequencies, the DC load line intersects the Y-Axis at VCC/RC. In our case, we split the theoretical RC across the real RC, RE1, and RE2.

RE1 provides additional protection from varying values of β by removing a dependency on internal emitter resistance in the 2N4401, and is thus chosen to be a small resistance of 20 Ω. RE2 ensures that the voltage at the collector is close to the center of our voltage range, which gives a good swing of voltage on the output.

For our third stage, based on the load line in Figure 8, RC is 600 Ω (15V / 25 mA). Splitting this value into 300 for the actual RC in our circuit, we select 20 Ω for RE1 and 280Ω for RE2.

The Q point chosen requires that VCE = 6.98V. The voltage at the collector is given by:

$$V_B = V_E + 0.7V$$
$$V_E = V_{CC} - I_C R_C - V_{CE}$$

From the above expression, VB=4.72 V. To correctly bias the base of the transistor, we choose RB1 and RB2 using the voltage divider principle, and using a general design rule:

$$\frac{V_{CC}}{R_{B1} + R_{B2}} \cong \frac{I_C}{10}$$

We select RB1 = 6700 Ω, and RB2 = 3300 Ω.

Having chosen the values for the components in this stage, we use Multisim to measure and check our bias conditions and assumptions. Current through a branch in Multisim can be measured by placing a 0 V DC source, and outputting the current

through the source using a DC operating point analysis. Figure 9 below shows the simulated DC operating point values of the circuit when constructed as described.

BJT Stage 3
DC Operating Point

	DC Operating Point	
1	vvc#branch	13.57642 m
2	vvb#branch	71.16192 u
3	$vc	10.92708
4	$vbb	4.79266
5	$ve	4.09427

In this table,
I_C is vvc#branch
I_B is vvb#branch
$vc is V_C
$vbb is V_{BB}
$ve is V_E

Figure 9. Stage 3 DC Operating Point Analysis

Input Impedance

The input impedance of common emitter BJT amplifier at sufficiently high frequencies is given by:

$$r_i = R_{B1} \| R_{B2} \| (r_\pi + (1+\beta_0) R_{E1})$$

Where rπ is defined as β0/gm, and β0 is the current gain at low frequencies. For the 2N4401, this parameter is provided in the datasheet as hFE. For the pre-laboratory calculations β0 is assumed to be 150.

The transconductance gm is given by IC/VT, where IC is the collector bias current and VT is the thermal voltage, or approximately 25 mA at room temperature.

Again, using the DC load line and the Q point, IC = 13mA, then rπ = 281Ω. From the expression for input resistance, and having selected all resistor values, we calculate ri to be approximately 1300Ω.

Gain

At sufficiently high frequencies, the emitter capacitor will act as a short to ground, and the voltage gain of the amplifier is given by:

$$A_v = \frac{-\beta_0 (R_C \| R_L)}{r_\pi + (1+\beta_0) R_{E1}}$$

Having determined all values in the above expression, we Av for the third stage is -10.9 V/V. This gain value is easily measured through simulation in Multisim. Using a virtual oscilloscope connected to the test circuit, we measure the gain in the completed simulated circuit to be -10.7 shown below in Figure 10. The small discrepancy is due to rounding error. Our hand calculations give a good estimate of the actual values, where as the simulation should be more accurate.

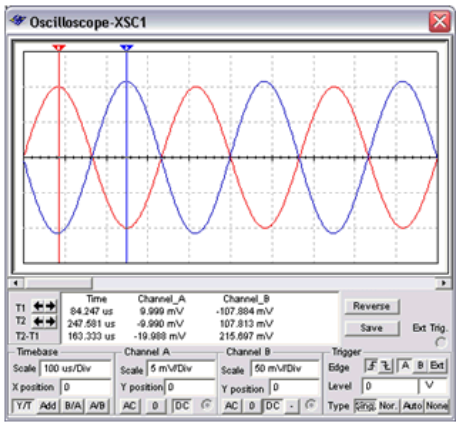


Figure 10. Simulated Results for Stage Three Gain Calculation

Capacitator Selection

The choice of capacitor values influences the frequency response of the amplifier. They must allow audio frequencies which range between around 80 Hz and 22 kHz. The values affect the time-constant of the amplifier.

The commonly used capacitor values of CE = 100 µF and CIN = COUT = 10 µF provide the appropriate AC characteristics.

The purpose of CIN is to isolate the small input signal from the DC bias voltages. The purpose of COUT is to provide the same isolation between stages, and between the last stage and output. The purpose of CE is to bypass the 2nd emitter resistance, creating a better path from the emitter to ground at higher frequencies.

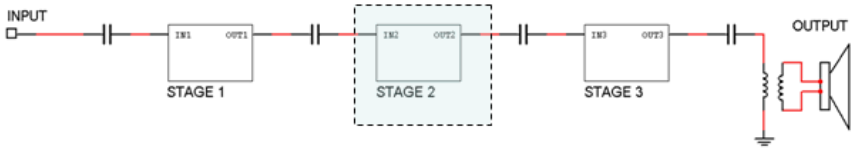
Summary

The values for stage 3 are as follows:

Description	Symbol	Value
DC Bias Base Current	I_B	70 uA
DC Bias Collector Current	I_C	13.34 mA
Collector-Emitter Voltage	V_{CE}	6.98 V
Collector Resistance	R_C	300 Ω
1st Emitter Resistance	R_{E1}	20 Ω
2nd Emitter Resistance	R_{E2}	280 Ω
Base Voltage Divider 1st Resistance	R_{B1}	6700 Ω
Base Voltage Divider 1st Resistance	R_{B2}	3300 Ω
Emitter bypass Capacitor	C_E	100 µF
Input and Output Capacitance	C_{IN}, C_{OUT}	10 µF
Voltage Gain (Absolute Value)	A_V	10.7 V/V
Input Resistance	r_i	1300 Ω
Load Resistance	R_L	1200 Ω

Table 1 - Salient Parameters of the Third Stage BJT Amplifier

4. BJT Amplifier, Stage 2



The second stage amplifier has the same topology as the third stage, with differing component values.

Since this application note details a real lab experiment taught in an institution, we deliberately omit the details of the second stage amplifier, and simply present the component values selected. The values for stage two are as follows:

Description	Symbol	Value
DC Bias Base Current	I_B	70 uA
DC Bias Collector Current	I_C	13.34 mA
Collector-Emitter Voltage	V_{CE}	6.98 V
Collector Resistance	R_C	150 Ω
1st Emitter Resistance	R_{E1}	20 Ω
2nd Emitter Resistance	R_{E2}	430 Ω
Base Voltage Divider 1st Resistance	R_{B1}	22 kΩ
Base Voltage Divider 1st Resistance	R_{B2}	22 kΩ
Emitter bypass Capacitor	C_E	100 µF
Input and Output Capacitance	C_{IN}, C_{OUT}	10 µF
Voltage Gain (Absolute Value)	A_V	6.1 V/V
Input Resistance	r_i	2472 Ω
Load Resistance - R_L of Stage 3	R_L	1309 Ω

Table 2. Salient Parameters of the Second Stage BJT Amplifier

5. JFET Stage

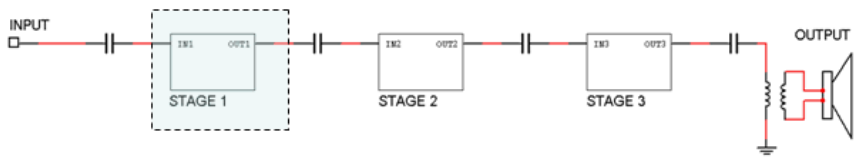


Figure 11 below gives the topology of the common source JFET amplifier.

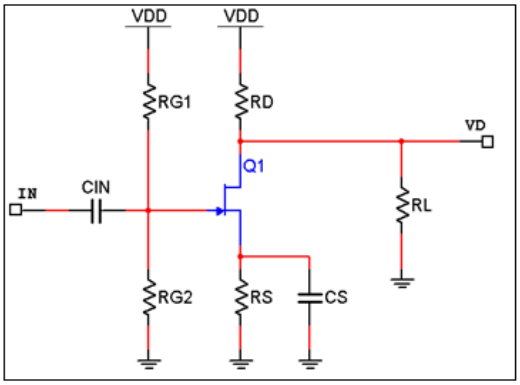


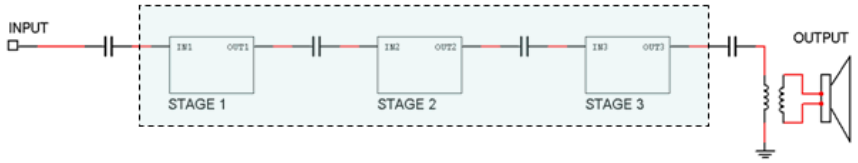
Figure 11 – Common Source JFET Amplifier Stage with Load Resistance

Again, we omit the details of the design of this stage to preserve the design challenge for students. Table 3 below gives the parameters chosen for the first stage.

Description	Symbol	Value
Gate Bias Resistance #1	R_{G1}	2 MΩ
Gate Bias Resistance #2	R_{G2}	2 MΩ
Input Resistance	r_i	1 MΩ
Gate Voltage	V_G	7.5 V
Drain Resistance	R_D	168 Ω
Source Resistance	R_S	1500 Ω
Input Capacitance	C_{IN}	10 µF
Source Capacitance	C_S	100 µF
Load Resistance	R_L	2594 Ω
Voltage Gain (Absolute Value)	A_V	2.2 V/V

Table 3 - Salient Parameters of the First Stage JFET Amplifier

6. System as a Whole



With each individual stage designed and simulated, we connect the pieces together and make (if necessary) adjustments to ensure that our design will provide the required characteristics. We also simulate the AC response of our design.

Figure 12 below shows the entire system gain. The gain is calculated to be 149.2 V/V which is within 0.5% of the design requirement of 150 V/V.

Figure 13 and Figure 14 below illustrate the magnitude and frequency response of the system as a whole. The magnitude response indicates a consistent gain across audible frequencies between 80 and 20 kHz.

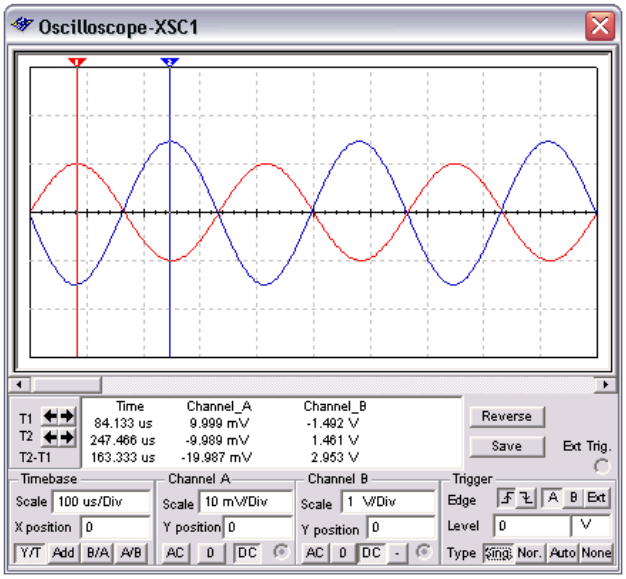


Figure 12 - System Gain

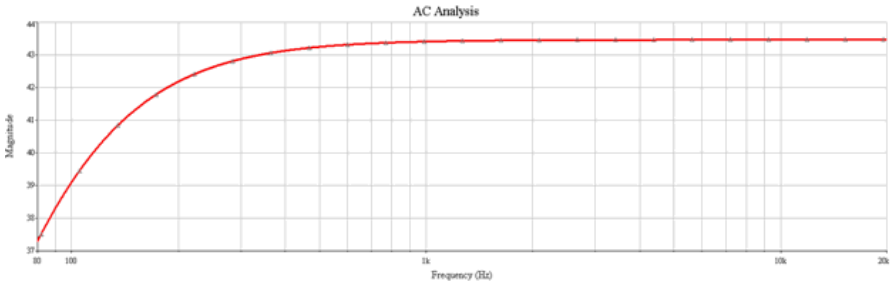


Figure 13 - System AC Magnitude Response (dB)

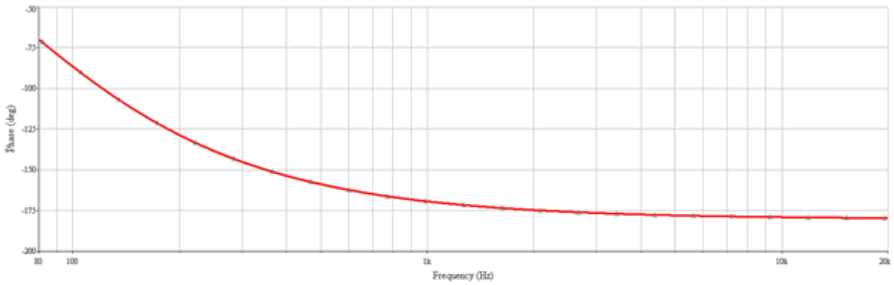


Figure 14 - System AC Phase Response (deg)

7. Virtual Prototyping and Prototyping with the NI ELVIS

Using the Virtual NI ELVIS prototyping environment ensures a smooth transition to a real-world prototype. By giving students a virtual representation of their circuit, they will be able to quickly understand how symbols relate to real world parts.

Multisim also provides a design rules check on virtually prototyped circuits, informing students of wiring errors, and saving valuable time in the lab. Once placed and wired on the 3D environment, components and nets will turn green, indicating success. This can be used as a double check for student wiring in the lab.

Tip: To create a virtual NI ELVIS schematic and corresponding breadboard, choose File/New/NI ELVIS Schematic. You can easily

copy and paste existing circuits into the NI ELVIS template.

Figure 15 and Figure 16 below show the 3D prototyped design, and the corresponding NI ELVIS schematic.

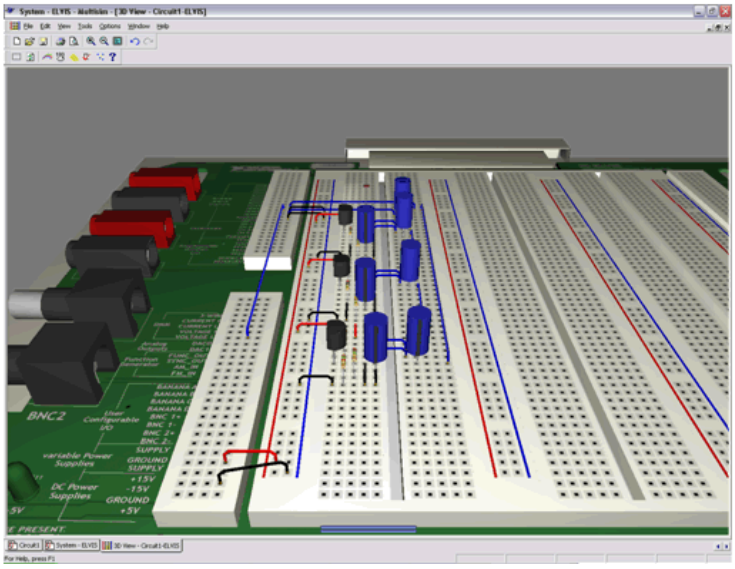


Figure 15 - 3D Virtual NI ELVIS Breadboard Showing Completed Prototype

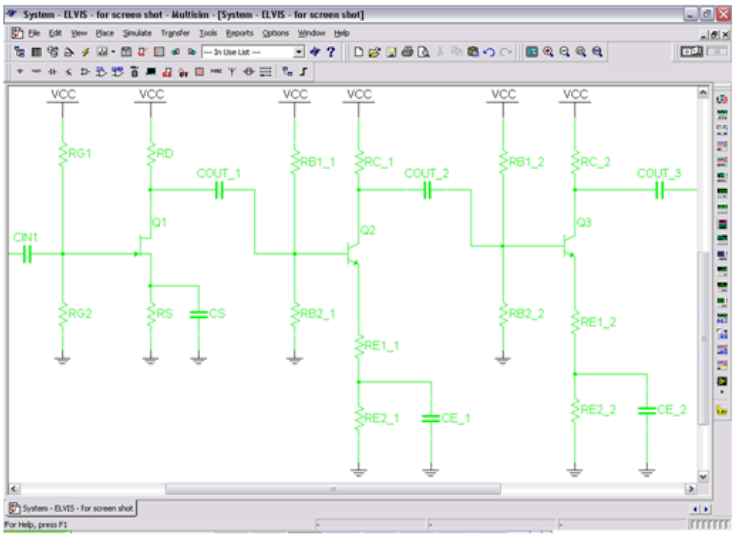
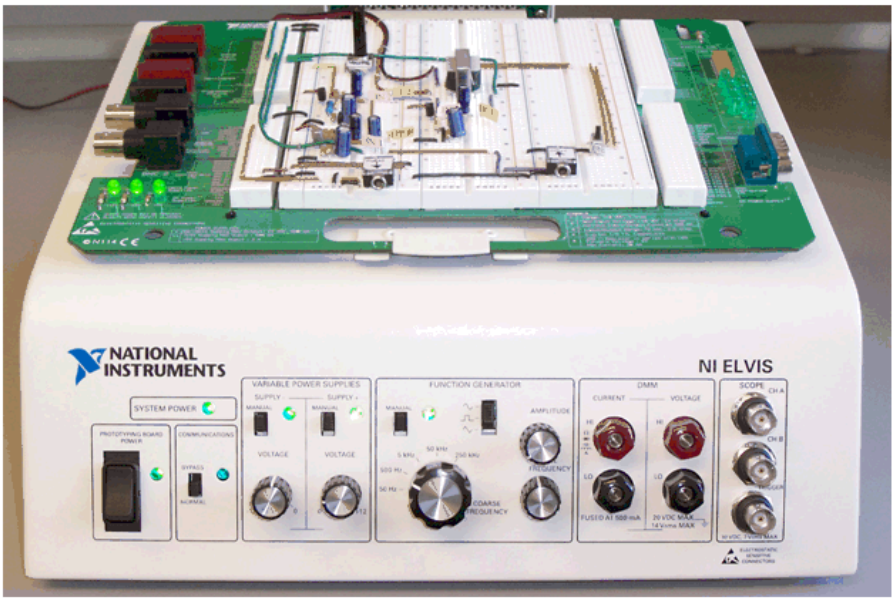


Figure 16 - NI ELVIS Schematic Showing Completed Design (Wires and Components are Green)

Prototyping with the NI ELVIS

We construct the complete circuit using real components on the NI breadboard.



Measurements

The NI ELVIS software front panels or virtual instruments are an excellent way to rapidly measure prototyped circuits.

Figure 17 and Figure 18 below show the gain measurements of the circuit using the NI ELVIS oscilloscope. Channel A (lower trace) in each case is the stimulus, and channel B (upper trace) in each case is the response.

The measured gain of the system is 144.39 V/V, which falls within 3.74 % of the required 150 V/V ±10 %.
Table 4 below gives a comparison of the simulated values and measured values

Parameter	Simulated	Measured	Percent Difference
Av Stage 1	2.2 V/V	2.10 V/V	4.5 %
Av Stage 2	6.1 V/V	6.05 V/V	0.82 %
Av Stage 3	10.7 V/V	11.6 V/V	-8.4 %
Av System	149.2 V/V	144.39 V/V	3.2 %

Table 4 - Comparison of Simulations to Measurements

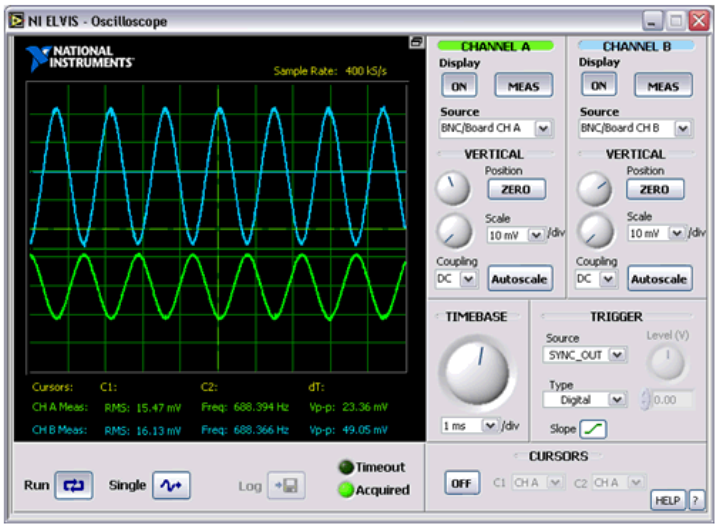


Figure 17 - Measured First Stage Gain

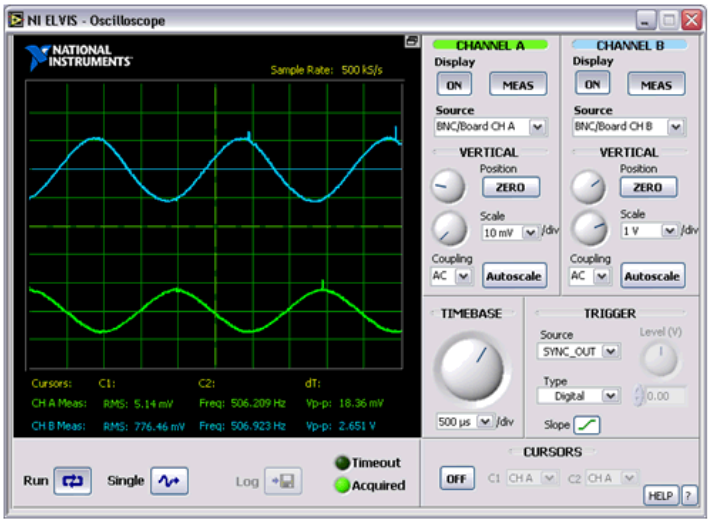


Figure 18 - Measured System Gain

Figure 19 illustrates the NI ELVIS Bode analyzer, which is used to measure the frequency response of the completed circuit.

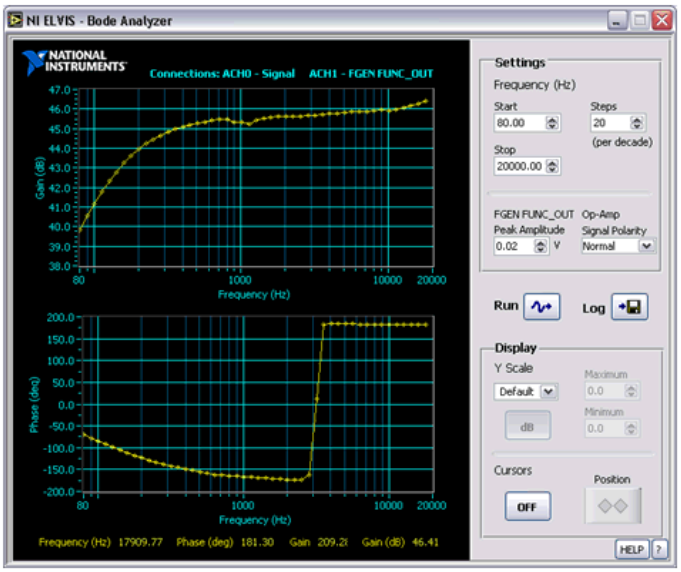


Figure 19 –Measured System Frequency Response

8. Comparing Simulations and Measurements

To compare our simulations with measurements we turn to National Instruments SignalExpress, an intuitive step-by-step measurement tool. SignalExpress is a simple and intuitive environment which allows users to easily configure measurements. SignalExpress also allows users to load Multisim simulation data. In Figure 20 below, we examine compare the simulated and measured gains of the system as a whole. SignalExpress, once configured correctly can automatically calculate percent differences.

The power of SignalExpress means that once students have set up their measurements, they can easily compare various iterations of their designs with one another. They can perform a series of tests on a given circuit easily without having to reconfigure their instruments. Simply by loading the particular workbench file into the SignalExpress environment the given measurement is ready to be executed.

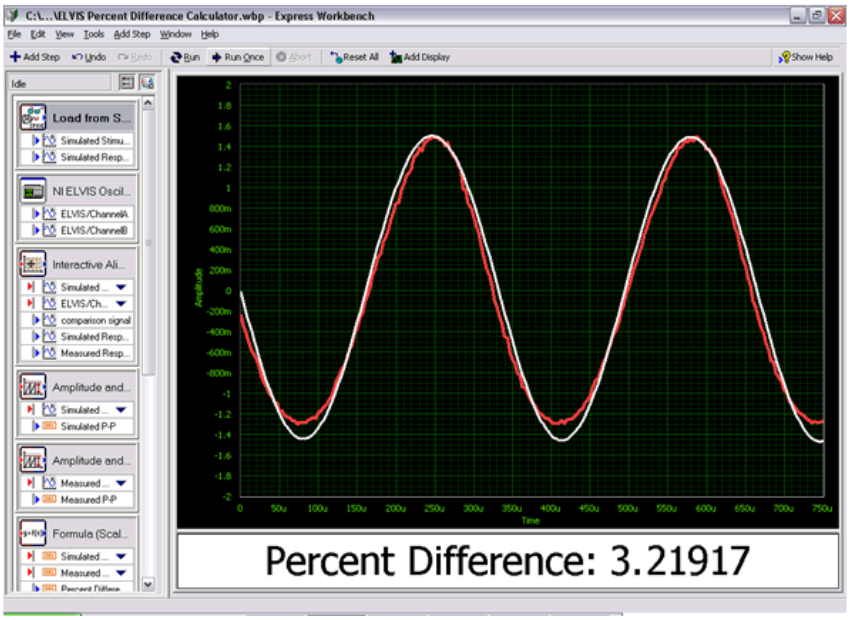
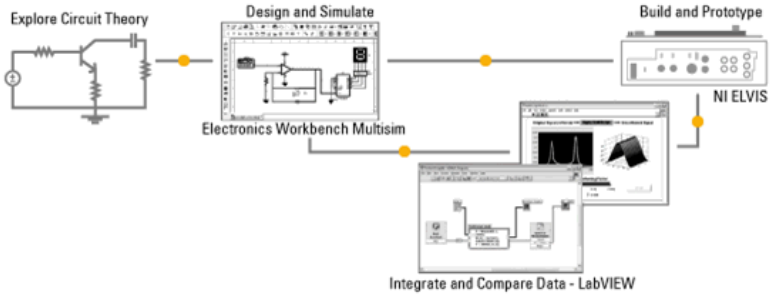


Figure 20 - Automatic Calculation of Percent Difference

9. Summary and Conclusions

Throughout the process of this design, the integrated laboratory helps us with intuitive simulation, and rapid measurements. Multisim is an invaluable tool for checking calculations experimenting with alternate designs, and provides a high degree of confidence before prototyping the circuit using real components. After prototyping the design on the NI ELVIS, powerful virtual instruments allow quick measurements of the relevant circuit characteristics. With NI SignalExpress we are able to directly compare results with simulations on the same screen.



See Also:

3-Hour Multisim Hands-On Instruction Manual (http://www.electronicsworkbench.com/email/intro_ms_3hr.zip)

Multisim Feature Demonstrations (http://www.electronicsworkbench.com/trymultisim)

View an Interactive Tutorial on the Integrated Platform for Electronics Education (https://sine.ni.com/apps/utf8/nigb.main?code=GB_TUTEWBCIRCUITS)

NI Academic Website (http://www.ni.com/academic)

Download LabVIEW (http://www.ni.com/trylabview) or evaluate online

Learn about NI SignalExpress (http://www.ni.com/signalexpress)

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2N4393 Silicon N-Channel Junction Field Effect Transistor, © 2006 Central Semiconductor http://www.ortodoxism.ro/datasheets/linearsystems/2N4391.pdf (http://www.ortodoxism.ro/datasheets/linearsystems/2N4391.pdf) (June 2006)

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